

INITIATIVE SIGNAL BHARAT REPORT 001 / SERIES I

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CLASSIFICATION PUBLIC — INDEPENDENT

INDIA'S NATIONAL DECISION STRESS-TEST

# The Chip That Could Break: *Five Structural Failure Points* India Hasn't Talked About

A rigorous stress-test of India's Semiconductor Mission — across time horizons, systems, and failure modes — examining what the official narrative is missing.

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OVERALL SIGNAL STATUS

● **Critical Warning**

FAILURE POINTS IDENTIFIED

**5**

**3–5 Years****₹1.6 Lakh Cr**

**Signal Bharat** — Independent Early Warning System for  
India's National Decisions

This report is independently produced. No institutional  
funding, no government affiliation, no advertiser. The  
analysis is the author's own.

§ 00 — PREMISE

## Why This Report Exists

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India is making one of the largest sovereign bets in its history. ₹1.6 lakh crore committed. A national mission. A Prime Minister personally inaugurating facilities. A target to produce chips for 70–75% of domestic needs by 2029.

The narrative is coherent, the momentum is real, and the ambition is legitimate. But momentum is not the same as resilience. Ambition is not the same as stress-tested strategy. And no independent, rigorous public analysis has yet asked the question that every high-stakes decision demands:

*"What are the specific, structural ways this can fail —  
and are we looking at them honestly?"*

This report does not argue that India's semiconductor mission will fail. It argues that five structural failure points have not been publicly examined with the seriousness they deserve — and that each one, left unaddressed, has the potential to undermine the entire stack.

The Signal Bharat Framework stress-tests decisions across three axes: **time horizons** (3-year / 10-year / 30-year), **systems** (economic, geopolitical, ecological, institutional), and **failure modes** (what breaks first, what breaks silently, what becomes irreversible). What follows is that analysis applied to India's semiconductor strategy.

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## § 01 — THE SIZE OF THE BET

# What India Has *Actually* Committed

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Before stress-testing a strategy, you must understand exactly what is at stake. The numbers here are larger — and more fragile — than the official narrative suggests.

**₹1.6 L Cr**

Total investment committed across 10 approved semiconductor projects as of March 2026

**50%**

Government subsidy coverage on eligible fabrication projects — meaning the state absorbs half the downside risk

**1 fab**

Number of silicon fabrication plants currently operational, against a target ecosystem of dozens

**90%**

India's current dependence on semiconductor imports — the baseline this mission must overcome

India's semiconductor market was valued at approximately \$45 billion in 2025, with a government target of \$100–110 billion by 2030. To sustain that trajectory, India must achieve growth rates in semiconductor manufacturing that *few countries have*

ever managed from a standing start. The historical record — Malaysia, Thailand, and others — is instructive and sobering.

The current approved portfolio includes two fabrication plants and eight assembly, testing, marking and packaging (ATMP/OSAT) facilities. The concentration in ATMP is itself a strategic vulnerability this report examines. The first commercially-made Indian chip — the Vikram 32-bit processor — was unveiled at SEMICON India 2025. A genuine milestone. But a 32-bit processor represents technology from the early 1990s by global standards. The distance between where India is and where the global frontier is cannot be papered over with ceremony.

This is not cynicism. It is calibration. The stress-test begins here.

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## § 02 — THE FIVE FAILURE POINTS

# What the *Mission Documents* Don't Stress-Test

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The following five structural failure points are not predictions of doom. They are the specific pressure points where India's semiconductor strategy is most vulnerable to cascade failure — and where current policy shows the least rigorous contingency thinking.

### FAILURE MODE 01 · STRUCTURAL

#### **The ATMP Trap: Assembly Without Sovereignty**

India's approved projects are overwhelmingly concentrated in assembly, testing, marking and packaging — the lowest-value, most commoditized segment of the

### FAILURE MODE 02 · DEPENDENCY

#### **The EDA Chokepoint: Software India Cannot Build Fast Enough**

Every chip India designs — from startup to government lab — currently runs on Electronic Design Automation software from three US

semiconductor value chain. This creates the illusion of a semiconductor industry while the actual intellectual property, design capability, and economic leverage remain entirely abroad. If global chip designers move to cheaper ATMP destinations (Vietnam, Malaysia, Mexico), India's entire investment thesis collapses without having built a single indigenous design capability.

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companies: Cadence, Synopsys, and Siemens. Together they control approximately 70% of the global EDA market. A US export restriction on EDA tools — already discussed in Washington policy circles regarding China — would not merely slow India's chip design industry. It would stop it entirely, overnight. India has no credible indigenous EDA development timeline that closes this gap within a decade.

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FAILURE MODE 03 ·  
GEOPOLITICAL

### **The Chinese Engineer Exodus: A Warning Already Triggered**

By July 2025, more than 300 Chinese engineers had left Foxconn's iPhone factories in India as part of a deliberate Chinese strategy to limit technology transfer to emerging competitors. This is not a random labor market event — it is a precedent. India's semiconductor ambitions depend on technology transfer from Taiwan, the US, and Japan. Each of these partnerships comes with competitive constraints, political conditions, and withdrawal risk that India's official strategy treats as fixed rather than fragile.

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FAILURE MODE 04 ·  
ECOLOGICAL

### **The Water Equation: Fabs Need What Gujarat May Not Have**

Semiconductor fabrication is among the most water-intensive industrial processes on earth. A single advanced fab can consume 10–15 million liters of ultra-pure water per day. India's primary semiconductor cluster is in Sanand, Gujarat — a region already under water stress. Gujarat's policy offers "discounted water tariffs" as an incentive. This is precisely backwards: it subsidizes the destruction of a resource that the fabs themselves require to survive. No public analysis has modeled what sustained semiconductor manufacturing does to Gujarat's water table over a 20-year horizon.

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FAILURE MODE 05 ·  
INSTITUTIONAL

### The Talent Pipeline Illusion: Numbers vs. Capability

India has over one million engineers skilled in software and AI. This is real. But semiconductor fabrication engineering — the discipline of actually building physical chips — is a completely different knowledge domain from software. The number of Indians specifically trained in semiconductor process engineering, materials science, and cleanroom operations is a small fraction of what the mission's scale requires. The C2S programme and DLI schemes are first-generation efforts that will not produce sufficient specialized talent before the Dholera fab requires it.

COMPOUNDING RISK

### The Cascade: When Two Failures Meet

The most dangerous scenario is not any single failure mode but their intersection. If EDA restrictions coincide with a water crisis in Gujarat's fab cluster, while the ATMP sector is being undercut by cheaper competitors in Southeast Asia — India faces three simultaneous pressures on a strategy with no clear fallback position. The mission documents do not model compound failure. This is the most significant gap in current strategic planning.

§ 03 — TIME HORIZON ANALYSIS

## How the Risk *Compounds* Over Time

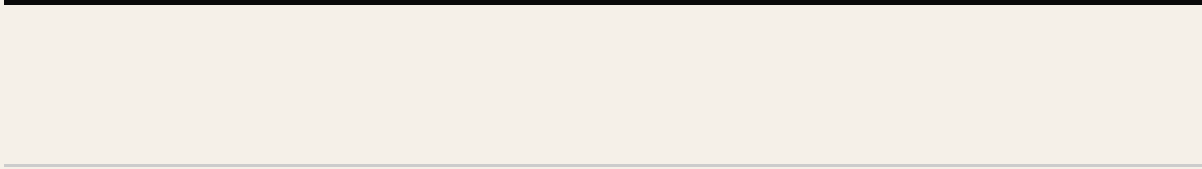
The Signal Bharat Framework maps each strategic decision across three time horizons to separate what is visible from what is structural.

HORIZON	WINDOW	WHAT WE'RE WATCHING	KEY RISK
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<b>Near-Term</b>	2026–2029	Can Tata's Dholera fab achieve commercial-scale production? Does Micron's ATMP facility deliver projected yield? Do the 50 targeted fabless startups under ISM 2.0 reach tape-out?	Execution slippage. India has no buffer — the political narrative has set expectations that cannot accommodate delay without damaging investor confidence.
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<b>Mid-Term</b>	2029–2036	Does India reach 3nm/2nm capability as targeted by ISM 2.0? Can India build a genuinely indigenous EDA capability? Does the ATMP sector face commoditization pressure from Southeast Asian competitors?	Technological stagnation at legacy nodes. India risks building world-class 28nm capacity precisely when the global market moves on — mirroring the trap China is trying to escape.
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<b>Long-Term</b>	2036–2055	Is India's chip design IP owned by Indians or by global primes? Does semiconductor manufacturing concentration in Gujarat survive climate-driven water stress? Has India produced a generation of genuine semiconductor scientists, or process operators?	Sovereignty without self-sufficiency. India may host fabs while the intellectual property, the process knowledge, and the economic surplus all flow outward. This is the historical pattern for every late entrant to manufacturing.
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THE BLIND SPOT

# The One Thing No One Is Saying Publicly

India's semiconductor strategy is, at its structural core, a geopolitical hedge strategy that has been packaged as an industrial policy. The actual goal — unstated but operationally real — is to give the US, Japan, and the Quad a credible alternative to Taiwan's TSMC concentration risk. India is not building a semiconductor industry for India. It is building a semiconductor insurance policy for the West.

This is not inherently wrong. But it carries a profound implication that current policy refuses to name: **India's leverage in this arrangement is temporary and declining.** The moment India's fabs are operational and the West's supply chain anxiety is reduced, India's negotiating position on technology transfer, on advanced node access, on IP ownership — weakens. The window to extract maximum concessions from global partners in exchange for geographic diversification is *right now*. India is not using it with sufficient strategic aggression.

Every month that passes without India demanding binding technology transfer agreements — not just investment commitments — as the price of its semiconductor real estate, is a month India leaves irreversible value on the table.

§ 05 — SIGNAL MATRIX

## India's Semiconductor Bets: *Current Status*

SIGNAL BHARAT — SEMICONDUCTOR SECTOR ASSESSMENT · MAY 2026

<p><b>ATMP / OSAT Buildout</b> (Gujarat cluster)</p>	<p><b>CAUTION</b></p>	<p>Operational. CG Semi, Micron, Kaynes Semicon producing. Risk: commoditization and value-chain ceiling.</p>
<p><b>Dholera Silicon Fab</b> (Tata + PSMC)</p>	<p><b>CAUTION</b></p>	<p>SEZ notified April 2026. Construction underway. Target node: 28nm. Risk: timeline slippage, node obsolescence on arrival.</p>

EDA Tool Sovereignty	WARNING	100% dependent on US EDA (Cadence, Synopsys, Siemens). No credible indigenous alternative in development. Single-point failure risk.
Semiconductor Talent Pipeline	WARNING	C2S programme active; 278 institutions, 72 startups. But fabrication-specific talent (process engineers, materials scientists) remains critically scarce.
Water Infrastructure for Fabs	WARNING	No public modelling of fab-cluster water demand against Gujarat groundwater capacity over 20-year horizon. Discounted tariff policy may accelerate depletion.
Indigenous Chip Design IP	CAUTION	Vikram processor milestone achieved. DLI funding 23 design projects. Gap: scale and commercial viability of indigenous IP remain unproven.
Technology Transfer Agreements	WARNING	No publicly available binding technology transfer terms from PSMC, Micron, or other partners. Investment ≠ knowledge transfer.
Geopolitical Dependency Risk (China)	WARNING	Chinese engineer withdrawal from Foxconn India already demonstrated willingness to weaponize labor. Rare minerals restriction pattern established.

## § 06 — WHAT WOULD CHANGE THE SIGNAL

# The *Four Actions* That Would Move This from Warning to Caution

Signal Bharat does not exist to criticize. It exists to identify exactly what would need to be true for the warning to be downgraded. Here

are the four concrete shifts that would substantively de-risk India's semiconductor strategy.

## **1. A National EDA Sovereignty Programme**

India should launch — with the urgency of a space mission — an indigenous EDA development programme, potentially housed within IIT Bombay, IISc, and C-DAC as a joint mandate. The target is not to match Cadence in five years. It is to have a credible, functional open-source EDA stack for legacy nodes (180nm–28nm) within three years, which is where India's immediate fabrication capacity lives. This de-risks the single most catastrophic external chokepoint in the entire strategy.

## **2. Mandatory Technology Transfer Covenants**

Every future ISM approval — every rupee of the 50% subsidy — should carry a legally binding technology transfer covenant: specific process knowledge, specific node capabilities, specific numbers of Indian engineers trained to a defined competency level. Investment without knowledge transfer is economic rent extraction by the foreign partner. India is paying for a semiconductor industry; it should demand one.

## **3. A Gujarat Fab Water Audit**

Commission an independent, public hydrogeological assessment of Gujarat's water table capacity against projected semiconductor cluster demand over a 20-year horizon. Publish the results. Build contingency infrastructure — water recycling mandates, alternative sourcing from the Narmada grid, and demand limits per fab — before the first large-scale fab is operational. The cost of this audit is trivial. The cost of discovering the problem in 2031 is not.

## **4. An ATMP Exit Strategy**

Acknowledge formally that ATMP is a transitional play, not a destination. Create explicit policy milestones at which India must have moved up the value chain to design and front-end fabrication. Without a sunset mechanism on ATMP subsidies

tied to design capability milestones, India risks locking in a low-value equilibrium that perpetuates dependency rather than resolving it.

SIGNAL BHARAT · REPORT 001 · END

# The Signal Is Clear. The Window Is Open.

India's semiconductor mission is not failing. But it is being built without the stress-testing infrastructure that decisions of this magnitude require. The five failure points identified in this report are all addressable — but only if they are named, mapped, and acted on before they become irreversible.

That is what Signal Bharat exists to do. Not to predict catastrophe. To make catastrophe less likely.

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Signal Bharat is an independent early warning system for India's national decisions.

Report 002 is in preparation. Topic: India's Power Grid Under EV Adoption Pressure.

For correspondence, collaboration, or Signal Contributor inquiries — contact the author directly.

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